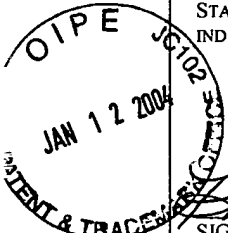


| CERTIFICATE OF MAILING VIA EXPRESS MAIL | |
|---|----------|
| PURSUANT TO 37 C.F.R. ' 1.10, I HEREBY CERTIFY THAT I HAVE A REASONABLE BASIS FOR BELIEF THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS EXPRESS MAIL POST OFFICE TO ADDRESSEE ON THE DATE INDICATED BELOW, AND IS ADDRESSED TO: | |
| MAIL STOP PATENT APPLICATION COMMISSIONER FOR PATENTS P.O. BOX 1450 ALEXANDRIA, VA 22313-1450 | |
|  SIGNATURE | DATE |

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Gordon Ma et al.Serial No.: **10/663,051**Filing Date: **September 15, 2003**Title: **LDMOS Transistor**

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Group Art Unit: **2811**

Examiner:

Attny. Docket No. **068736.0232**Client Ref.: **2003P52735US**

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicants respectfully request, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the art listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. A copy of the cited art is enclosed for the convenience of the Examiner.

Furthermore, pursuant to 37 C.F.R. §§1.97(g) and (h), no representation is made that these references are material to the patentability of the present application.

As the Information Disclosure Statement is being submitted before the mailing of the first office action on the merits, Applicants believe that no fee is required. If a fee is

required, please accept this transmittal as a petition therefor and charge any fee to Baker Botts L.L.P. (*formerly, Baker & Botts, L.L.P.*) Deposit Account No. 02-0383, Order No. (068736.0232) for any other charges necessary for the filing of this Information Disclosure Statement.

Date: January 12, 2004

BAKER BOTTS L.L.P. (023640)

By: 

Andreas H. Grubert

(Limited recognition 37 C.F.R. §10.9)

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AGENT FOR APPLICANTS

PTO-1449

Application No.
10/663,051Applicant(s):
GORDON MA ET AL.Information Disclosure Citation
in an ApplicationDocket Number
068736.0232Group Art Unit
2811Filing Date
September 15, 2003

U.S. PATENT DOCUMENTS

| | DOCUMENT NO. | DATE | NAME | CLASS | SUBCLASS | FILING DATE |
|---|--------------|----------|-----------------|-------|----------|-------------|
| 1 | 4,811,075 | 03/07/89 | Eklund | 357 | 46 | 04/24/87 |
| 2 | 5,155,563 | 10/13/92 | Davies et al. | 357 | 23.4 | 03/18/91 |
| 3 | 5,313,082 | 05/17/94 | Eklund | 257 | 262 | 02/16/93 |
| 4 | 6,168,983 | 01/02/01 | Rumennik et al. | 438 | 188 | 02/05/99 |
| 5 | 6,563,171 | 05/13/03 | Disney | 257 | 342 | 11/12/02 |

FOREIGN PATENT DOCUMENTS

| | DOCUMENT NO. | DATE | COUNTRY | CLASS | SUBCLASS | TRANSLATION | |
|--|--------------|------|---------|-------|----------|-------------|----|
| | | | | | | YES | NO |
| | | | | | | | |
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NON-PATENT DOCUMENTS

| | DOCUMENT (Including Author, Title, Source, and Pertinent Pages) | DATE |
|----|---|------|
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| 7 | H.M.J. Vaes and J.A. Appels, "High voltage high current lateral devices", IEDM technical digest, pp. 87-90 | 1980 |
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EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.